REMARKS

I. Amendment to the Specification

It was requested that Applicants update the application number of the commonly assigned US Patent Application to Vyvoda et al. Applicants have amended paragraph [0030] on page 10 at line 33 to make the requested change.

II. Amendments to the Claims

To clarify the claims, Applicants have amended independent claim 1 to recite that the semiconductor regions of the wafer are formed over a substrate. Independent claim 30 has been amended to recite that the means for repelling water from the surface of the claimed wafer comprise regions above a substrate. Independent claim 44 has been amended to recite that the hydrophobic regions exposed at the wafer surface are deposited over a substrate. In Lee, the reference cited by the Examiner, the semiconductor regions, water repelling means, and hydrophobic regions are formed in the semiconductor substrate itself (column 4, lines 50-59, and Fig. 4E.) These amendments were made merely to clarify the claims and were not made for purposes of patentability. As discussed in detail below, the rejections set forth in the Office Action are improper; accordingly the present amendments are not necessary to overcome the rejections.

III. Claim Rejections

Independent claims 1, 30, and 44 were rejected under 35 USC 102.

A. Claim Rejection 35 US 102, Claim 1 and Dependents

Independent claim 1 and its dependent claims 6-12 and 14 have been rejected under 35 USC 102(e) as being anticipated by Lee et al., U.S. Patent No. 6,258,696.

Applicants respectfully traverse these rejections because Lee fails to disclose each and every element recited in independent claim 1.

Claim 1 recites a wafer having a surface, the wafer comprising:

> a plurality of regions of semiconductor and dielectric exposed at the surface of the wafer after chemical mechanical planarization, wherein
>
> the semiconductor regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and
>
> each of the semiconductor regions have a shortest surface dimension that is less than or equal to a first width,
>
> **the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.**

The Examiner notes that the expressions "after chemical planarization" and "allowing removal of residual particles therefrom" are "taken to be ... product by process limitation[s] and [are] given no patentable weight." The Examiner further notes "it is the patentability of the final structure of the product 'gleaned' from the process steps, which must be determined in a 'product by process' claim, and not the patentability of the process."

The Examiner is correct that the phrase "after chemical mechanical planarization" describes part of the process used to create the wafer claimed in claim 1. The phrase "allowing removal of residual particles therefrom", however, does not describe part of the process of creating the wafer.

Recall that the invention relates to wet cleaning of wafer surfaces following chemical mechanical planarization (CMP). An aqueous cleaning technique is conventionally used to remove residual slurry particles from a silicon dioxide dielectric surface following CMP and to remove residual slurry particles from a combined silicon dioxide and silicon nitride dielectric surface following shallow trench isolation (STI) planarization. Both silicon dioxide and silicon nitride are hydrophilic. However, when silicon is exposed following a CMP process, a hydrophobic (i.e., water-repelling) surface is created, which makes it difficult to use aqueous NH_4OH-based scrubbing. The silicon surface does not sufficiently wet to permit the polyvinyl alcohol brushes coming into intimate contact with the wafer surface, and the residual slurry particles and/or metal contaminants are not removed.

An object of the invention, then, is to provide a wafer surface comprising semiconductor and dielectric that attracts enough water to allow the wafer surface to wet so that residual slurry particles and metal contaminants may be removed therefrom. The invention is not a wafer surface that has been cleaned, but rather one that is cleanable. Thus the entire phrase, "the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom" specifies not the process used to make the wafer, but rather a property the wafer, "the product 'gleaned' from the process steps" referred to by the Examiner above, must have. The property defined by this phrase, therefore, is a crucial limitation to the claim, and must in fact be given patentable weight.

Lee apparently teaches alternating lines of semiconductor substrate 402' and insulation film 403 planarized by CMP or an etch-back process (column 4, lines 50-59.)

But the reference fails to recognize the difficulty of cleaning such a surface following CMP. It gives no guidance regarding the relative widths of the lines of semiconductor substrate 402' and the lines of insulation film 403, and nowhere suggests or teaches that the semiconductor region fraction of the wafer surface, or the width of any semiconductor region, must be selected to ensure that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

It should be noted that the property of being cleanable described by the noted limitation cannot be presumed to be inherent. To assume the relative widths of the lines of semiconductor substrate 402' and the lines of insulation film 403 from a subjective estimate of their appearance in figures, in the absence of an explicit teaching, is improper. "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ 2D (BNA) 1746, 1749 (Fed. Cir. 1991.) "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981.)

Because Lee fails to teach each and every element recited in independent claim 1, Applicants request that the 35 U.S.C. § 102(e) rejections of independent claim 1 and its dependent claims be withdrawn.

B. Claim Rejection 35 US 102, Claim 30 and Dependents

Independent claim 30 and its dependent claims 35-41 and 43 have been rejected under 35 USC 102(e) as being anticipated by Lee. Applicants respectfully traverse these rejections because Lee fails to disclose each and every element recited in independent claim 30.

Claim 30 recites a wafer having a surface, the wafer comprising:

means for attracting water to the surface of the wafer; and

means for repelling water from the surface of the wafer comprising regions that have a combined surface area that is less than or equal to a first fraction of a surface area of the wafer,

wherein each of the regions has a shortest surface dimension that is less than or equal to a first width, and **the first fraction and the first width ensure that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.**

As noted above, Lee fails to recognize the difficulty of cleaning such a surface following CMP. It gives no guidance regarding the relative widths of the lines of means for repelling water (402') and the lines of means for attracting water (403), and nowhere suggests or teaches that the fraction of the wafer surface comprising means for repelling water from the surface of a wafer, or the width of regions of such means, must be selected to ensure that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

Because Lee fails to teach each and every element recited in independent claim 30, Applicants request that the 35 U.S.C. § 102(e) rejections of independent claim 30 and its dependent claims be withdrawn.

C. Claim Rejection 35 US 102, Claim 44 and Dependents

Independent claim 44 and its dependent claims 49-54 and 56 have been rejected under 35 USC 102(e) as being anticipated by Lee. Applicants respectfully traverse these rejections because Lee fails to disclose each and every element recited in independent claim 1.

Claim 44 recites a wafer having a surface, the wafer comprising:

> a plurality of regions of hydrophobic material and hydrophilic material exposed at the surface of the wafer after chemical mechanical planarization, wherein the regions of hydrophobic material have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and each of the regions of hydrophobic material have a shortest surface dimension that is less than or equal to a first width, **the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.**

As noted above, Lee fails to recognize the difficulty of cleaning such a surface following CMP. It gives no guidance regarding the relative widths of the lines of hydrophobic material (402') and the lines of hydrophilic material (403), and nowhere suggests or teaches that the fraction of the wafer surface comprising hydrophobic material, or the width of regions of hydrophobic material, must be selected to ensure that

the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

Because Lee fails to teach each and every element recited in independent claim 44, Applicants request that the 35 U.S.C. § 102(e) rejections of independent claim 44 and its dependent claims be withdrawn.

D. Claim Rejections 35 USC 103, Dependent Claims

Claims 2-5, 31-34, and 45-48 have been rejected under 35 USC 103(a) as being unpatentable over Lee. Claims 13, 42, and 55 have been rejected under 35 USC 103(a) as being unpatentable over Lee in view of Inoue.

All of these claims depend from either claim 1, 30, or 44, the rejections of which were discussed in sections A, B, and C. Lee fails to teach each and every element recited in any of these independent claims, and so clearly fails to teach each and every element recited in the dependent claims as well. Applicants request that the 35 U.S.C. § 103(a) rejections of these dependent claims be withdrawn.

IV. Conclusion

In view of these amendments and remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. **If any objections or rejections remain, Applicants respectfully request an interview to discuss the references.** In such event, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

January 14, 2003

Date

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APPENDIX A

Paragraph [0030] on page 10, line 33:

Now as shown in FIG. 2F, the spaces between the semiconductor regions 25A and 25B are filled with a dielectric layer 26 (e.g., SiO.sub.2), which may be formed with a high density plasma chemical vapor deposition (HDP-CVD) process. The dotted line in FIG. 2F indicates that dielectric layer 26 is filled to any suitable height, including above the upper edge of semiconductor regions 25A and 25B. Preferably, dielectric layer 26 is filled up to and no higher than the upper edge of the semiconductor regions to minimize the amount of subsequent planarization needed. This tends to minimize non-uniformities across the entire wafer. Further details of this technique are discussed in commonly-assigned U.S. patent application Ser. No. 09/776,000, pending, to Vyvoda et al., filed concurrently herewith, [(Attorney Docket No. MS-2),] which is hereby incorporated by reference herein in its entirety.

APPENDIX B

1. (Amended) A wafer having a surface, the wafer comprising:

a plurality of regions of semiconductor and dielectric exposed at the surface of the wafer after chemical mechanical planarization, the semiconductor regions formed over a substrate, wherein

the semiconductor regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and

each of the semiconductor regions have a shortest surface dimension that is less than or equal to a first width,

the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

30. (Amended) A wafer having a surface, the wafer comprising:

means for attracting water to the surface of the wafer; and

means for repelling water from the surface of the wafer comprising regions above a substrate that have a combined surface area that is less than or equal to a first fraction of a surface area of the wafer,

wherein each of the regions has a shortest surface dimension that is less than or equal to a first width, and the first fraction and the first width ensure that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

44. (Amended) A wafer having a surface, the wafer comprising:

a plurality of regions of hydrophobic material and hydrophilic material exposed at the surface of the wafer after chemical mechanical planarization, wherein the regions of hydrophobic material are deposited over a substrate and have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer, and each of the regions of hydrophobic material have a shortest surface dimension that is less than or equal to a first width, the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

PTO/SB/96 (08-00)
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Michael A. Vyvoda

Application No./Patent No.: 09/776009 Filed/Issue Date: February 2, 2001

Entitled: Wafer Surface that Facilitates Particle Removal

MATTIX SEMICONDUCTOR, a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☐ the assignee of the entire right, title, and interest; or
2. ☑ an assignee of less than the entire right, title and interest.
The extent (by, percentage) of its ownership interest is 50 %

in the patent application/patent identified above by virtue of either:

A. [✓] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached. 012673 0648

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From:_____ To:_____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame_____, or for which a copy thereof is attached.

2. From:_____ To:_____
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[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.
[NOTE: A separate copy (*i.e.*, the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

December 16, 2002
Date

Liza K. Toth, Reg#31,065
Typed or printed name

Liza K. Toth
Signature

Vice President, IP
Title

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Michael A. Vyvoda

Application No./Patent No.: 09/776009 Filed/Issue Date: February 2, 2001

Entitled: Water Surface that Facilitates Particle Removal

LSI Logic (Name of Assignee) , a Corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.),

states that it is:

1. ☐ the assignee of the entire right, title, and interest; or
2. ☑ an assignee of less than the entire right, title and interest.
The extent (by, percentage) of its ownership interest is 50 %

in the patent application/patent identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

012673 0648

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

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The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame_____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.
[NOTE: A separate copy (*i.e.*, the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

December 16, 2002
Date

Timothy R. Croll
Typed or printed name

Timothy R Croll
Signature

Senior Corporate Counsel, IP Reg#36,771
Title